WHAT IS CLAIMED IS:

1. A system for managing circuit emulation service over an Asynchronous Transfer Mode (ATM) network, comprising:

control logic configured to receive channelized circuit data, the channelized circuit data being transmitted at an arbitrary rate;

control logic configured to format the channelized circuit data into one or more ATM cells, each ATM cell having a payload, the payload having a plurality of octets and corresponding validity fields, each validity field indicating whether the associated octet contains valid data; and

control logic configured to transmit the one or more ATM cells across the ATM network;

wherein the transmission of the one or more ATM cells effectively results in transmission of the channelized circuit data at the arbitrary rate over the ATM network; and

wherein the arbitrary rate is not a multiple of a fundamental rate.

2. The system of claim 1 wherein the arbitrary rate is less than the fundamental rate.

3. The system of claim 1 wherein the arbitrary rate is higher than the fundamental rate.

4. Traffic aggregation equipment incorporating the system as recited in claim 1.

5. A system for managing circuit emulation service over an Asynchronous Transfer Mode (ATM) network, comprising:

a first ATM processor configured to:

receive channelized circuit data, the channelized circuit data being transmitted at an arbitrary rate;

format the channelized circuit data into one or more ATM cells, each ATM cell having a payload, the payload having a plurality of octets and corresponding validity fields, each validity field indicating whether the associated octet contains valid data; and

transmit the one or more ATM cells across the ATM network; and

a second ATM processor configured to receive and process the one or more ATM cells transmitted from the first ATM processor;

wherein the transmission of the one or more ATM cells effectively results in transmission of the channelized circuit data at the arbitrary rate over the ATM network; and

wherein the arbitrary rate is not a multiple of a fundamental rate.

6. The system of claim 5 wherein the second ATM processor processes each ATM cell based on the validity fields and the associated octets contained therein;

wherein if a validity field indicates a "valid" status, the associated octet is considered to be containing valid data and will be processed, and if the validity field indicates an "invalid" status, the associated octet is considered to be containing invalid data and will not be processed; and

wherein by processing the one or more ATM cells based on the validity fields contained therein, the transmission of the one or more ATM cells effectively results in transmission of the channelized circuit data at the arbitrary rate over the ATM network.

7. The system of claim 5 wherein the arbitrary rate is less than the fundamental rate.

8. The system of claim 5 wherein the arbitrary rate is higher than the fundamental rate.

9. A method for managing circuit emulation service over an Asynchronous Transfer Mode (ATM) network, the method comprising:

receiving channelized circuit data, the channelized circuit data being transmitted at an arbitrary rate;

formatting the channelized circuit data into one or more ATM cells, each ATM cell having a payload, the payload having a plurality of octets and corresponding validity fields, each validity field indicating whether the associated octet contains valid data; and

transmitting the one or more ATM cells across the ATM network;

wherein the transmission of the one or more ATM cells effectively results in transmission of the channelized circuit data at the arbitrary rate over the ATM network; and

wherein the arbitrary rate is not a multiple of a fundamental rate.

10. The method of claim 9 wherein the arbitrary rate is less than the fundamental rate.

11. The method of claim 9 wherein the arbitrary rate is higher than the fundamental rate.

12. A method for managing circuit emulation service over an Asynchronous Transfer Mode (ATM) network, the method comprising:

directing a first ATM processor to:

receive channelized circuit data, the channelized circuit data being transmitted at an arbitrary rate;

format the channelized circuit data into one or more ATM cells, each ATM cell having a payload, the payload having a plurality of octets and corresponding validity fields, each validity field indicating whether the associated octet contains valid data; and

transmit the one or more ATM cells across the ATM network; and

directing a second ATM processor to receive and process the one or more ATM cells transmitted from the first ATM processor;

wherein the transmission of the one or more ATM cells effectively results in transmission of the channelized circuit data at the arbitrary rate over the ATM network; and

wherein the arbitrary rate is not a multiple of a fundamental rate.

13. The method of claim 12 further comprising:

directing the second ATM processor to process each ATM cell based on the validity fields and the associated octets contained therein;

wherein if a validity field indicates a "valid" status, the associated octet is considered to be containing valid data and will be processed, and if the validity field indicates an "invalid" status, the associated octet is considered to be containing invalid data and will not be processed; and

wherein by processing the one or more ATM cells based on the validity fields contained therein, the transmission of the one or more ATM cells effectively results in transmission of the channelized circuit data at the arbitrary rate over the ATM network.

14. The method of claim 12 wherein the arbitrary rate is less than the fundamental rate.

15. The method of claim 12 wherein the arbitrary rate is higher than the fundamental rate.